REMARKS

In the Office Action, the Examiner noted that claims 1-20 are pending in the application and that claims 1-20 are rejected. By this response, claims 1-2, 4, and 11-19 are amended. Claims 3 and 5 are cancelled. In view of the above amendments and the following discussion, Applicants submit that none of the claims now pending in the application are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Thus, Applicants believe that all of these claims are now in condition for allowance.

I. Rejection of Claims Under 35 U.S.C. §102(b)

The Examiner rejected claims 1-2, 4, and 6-20 as being anticipated by Jyu et al. (U.S. Patent 5,880,967, issued March 9, 1999) ("Jyu"). The rejection is respectfully traversed.

More specifically, the Examiner stated that Jyu teaches designing an integrated circuit in accordance with timing constraint data using a timing-driven design process to produce a design result optimized for timing performance and not for power consumption. (Office Action, pp. 2-3). The Examiner further stated that Jyu teaches identifying logic paths that have a timing characteristic within a threshold to define first and second logic paths, and selectively optimizing the integrated circuit to reduce power consumption in response to the first and second logic paths. (Office Action, p. 4). The Examiner concluded that Jyu anticipates Applicants' invention of claim 1.

Jyu teaches minimizing signal delay and power consumption by iteratively resizing transistors in a design. (Jyu, Abstract). A transistor resizer processes a circuit netlist and can operate in a requirement mode, a cost function mode, or a slack-driven mode. In the requirement mode, the engine first satisfies a specified delay and then minimizes for power. (Jyu, col. 10, lines 56-67).

Jyu, however, does not teach each and every element of Applicants' invention recited in amended claim 1. Namely, Jyu does not teach or suggest designing an integrated circuit to produce a result optimized for only timing and then selectively performing synthesis, mapping, placing, and routing of the integrated circuit to reduce power consumption. Rather, Jyu discloses adjusting transistor size in a circuit netlist.

Jyu is devoid of any disclosure regarding implementation of the netlist, including synthesis, mapping, placing, and routing the design for an integrated circuit to reduce power consumption.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 221 USPQ 481, 485 (Fed. Cir. 1984) (emphasis added). Since Jyu does not teach designing an integrated circuit to produce a result optimized for only timing and then selectively performing synthesis, mapping, placing, and routing of the integrated circuit to reduce power consumption, Jyu does not teach each and every element of Applicants' invention recited in claim 1. Thus, Jyu does not anticipate Applicants' invention recited in claim 1.

Independent claims 11, 14, and 17 each recite features similar to the features of claim 1 emphasized above. For the same reasons discussed above, Applicants contend that claims 11, 14, and 17 are not anticipated by Jyu. Claims 2, 4, 6-10, 12-13, 15-16, and 18-20 depend from claims 1, 11, 14, and 17 and recite additional features therefor. Since Jyu does not anticipate Applicants' claims 1, 11, 14, and 17, Jyu also fails to anticipate claims 2, 4, 6-10, 12-13, 15-16, and 18-20.

In view of the foregoing, Applicants contend that claims 1-2, 4, and 6-20 are not anticipated by Jyu and, as such, fully satisfy the requirements of 35 U.S.C. §102. Accordingly, Applicants respectfully request that the present rejection be withdrawn.

II. Rejection of Claims Under 35 U.S.C. § 103(a)

The Examiner rejected claims 3 and 5 as being unpatentable over Jyu in view of Chen (U.S. Patent 6,687,888, issued February 3, 2004). The rejection is respectfully traversed.

More specifically, the Examiner conceded that Jyu does not teach placing logic and routing connections. (Office Action, p. 7). The Examiner stated, however, that Chen teaches power optimization having placement and routing processes. (Office Action, p. 7). The Examiner concluded that it would have been obvious to employ the power optimization process of Chen with the transistor resizing process of Jyu. (Office

Action, pp. 7-8). Applicants respectfully disagree.

Claims 3 and 5 have been cancelled. Claim 1 has been amended to include features similar to those of claims 3 and 5. Namely, claim 1 as amended recites a step of selectively performing synthesis, mapping, placing, and routing of the integrated circuit to reduce power consumption in response to said first set of logic paths and said second set of logic paths. The cited references, either singly or in any permissible combination, do not teach, suggest, or otherwise render obvious Applicants' invention recited in claim 1.

In particular, as discussed above, Jyu is devoid of any teaching or suggestion of implementing the circuit netlist, including steps of synthesis, mapping, placing, and routing the design for an integrated circuit to reduce power consumption. Chen discloses that timing and power are optimized simultaneously to produce an optimized design result. (Chen, col. 8, line 30-67; FIG. 3A; col. 9, lines 1-62; FIG. 4; col. 11, line 32 to col. 12, line 19; FIG. 6). Thus, placement and routing in Chen is performed such that timing and power are optimized simultaneously. Chen does not teach or suggest synthesizing, mapping, placing, and routing an integrated circuit to deduce power consumption. Since neither Jyu nor Chen teaches or suggests such a feature, no conceivable combination of Jyu and Chen renders obvious Applicants' invention of claim 1. Therefore, Applicants contend that claim 1 is patentable over the cited combination and, as such, fully satisfies the requirements of 35 U.S.C. §103.

CONCLUSION

Thus, Applicants submit that none of the claims presently in the application are anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Consequently, Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring any adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Michael R. Hardaway at (408) 879-6149

so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on January 5, 2007.

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